STATUS OF THE CLAIMS

Claims 1-39 (Canceled).

40. (Previously presented) A semiconductor device comprising:

a semiconductor structure having at least one metal contact layer formed on a surface thereof;

a first insulator layer formed on said at least one metal contact layer;

at least one metal pad overlying said first insulator layer and in contact with said at least one metal contact layer;

a second insulator layer formed on said at least one metal pad and at least a portion of said first insulator layer; and,

at least one solder contact ball formed in the second insulator layer and in contact with said at least one metal pad, said at least one solder contact ball having a diameter less than 100 microns.

Claims 41-42 (Canceled).

43. (Previously presented) The semiconductor device of claim 40, wherein said at least one solder contact ball has a diameter less than 10 microns.

44. (Previously presented) The semiconductor device of claim 40, wherein said at least one solder contact ball has a diameter of approximately 2 microns.

45. (Previously presented) The semiconductor device of claim 40, wherein said at least one metal contact layer is connected to said at least one metal pad by a via hole formed in the first insulator layer.

46. (Previously presented) The semiconductor device of claim 40, wherein the at least one solder contact ball extends from a top surface of the second insulator layer to the metal pad by a through-hole formed in the second insulator layer.

47. (Previously presented) The semiconductor device of claim 40, wherein the at least one metal pad lies at least partially overtop of the at least one metal contact layer.

48. (Original) The semiconductor device of claim 40, wherein the semiconductor device is an integrated circuit chip.

49. (Original) The semiconductor device of claim 40, wherein the semiconductor device is an integrated circuit wafer.

50. (Original) The semiconductor device of claim 40, wherein the semiconductor device is bonded to a module substrate.

51. (Original) The semiconductor device of claim 40, wherein the semiconductor device is bonded to a circuit board.

Claims 52-67 (Canceled).

68. (Previously presented) The semiconductor device of claim 40, wherein said first insulator layer is at least 2 microns thicker than said at least one metal contact layer.

69. (Original) The semiconductor device of claim 40, wherein said metal pad comprises a metal stack comprising four different metal levels.

70. (Original) The semiconductor device of claim 69, wherein said metal levels comprise Zirconium, Nickel, Copper and Gold.

71. (Previously presented) A semiconductor device formed on a semiconductor substrate having at least one metal contact layer formed thereon, said semiconductor device comprising:

a first insulating layer formed over and in contact with said at least one metal contact layer; and

at least one solder contact ball formed in the first insulating layer, wherein said at least one solder contact ball has a diameter between 2 and 100 microns.

72. (Previously presented) The semiconductor device of claim 71, wherein said at least one solder contact ball has a diameter of approximately 2 microns.

73. (Canceled).

74. (Previously presented) The semiconductor device of claim 40, wherein said at least one solder contact ball has a diameter less than 50 microns.

75. (Previously presented) The semiconductor device of claim 40, wherein said at least one solder contact ball has a diameter less than 25 microns.

76. (Previously presented) A semiconductor device comprising:

a semiconductor structure having at least one metal layer formed over a surface thereof;

a first insulating layer formed over said at least one metal layer, wherein said first insulating layer is at least two microns thicker than said at least one metal layer;

at least one metal stack formed over said first insulating layer and in contact with said at least one metal layer;

a second insulating layer formed over said at least one metal stack; and,

an etched solder layer having a thickness of at least 2.33 microns, wherein said etched solder layer forms at least one solder contact in said second insulating layer and in contact with said at least one metal stack.

77. (Previously presented) The semiconductor device of claim 76, wherein said at least one solder contact has a diameter from 2 microns to 100 microns.

78. (Previously presented) The semiconductor device of claim 77, wherein said at least one solder contact has a diameter less than 50 microns.

79. (Previously presented) The semiconductor device of claim 78, wherein said at least one solder contact has a diameter less than 25 microns.

80. (Previously presented) The semiconductor device of claim 79, wherein said at least one solder contact has a diameter less than 10 microns.

81. (Previously presented) The semiconductor device of claim 79, wherein said at least one solder contact has a diameter of approximately 2 microns.

82. (Previously presented) The semiconductor device of claim 76, wherein said at least one metal stack is formed of at least three different metals.

83. (Previously presented) The semiconductor device of claim 82, wherein said three different metals are zirconium, nickel, and copper.

84. (Previously presented) The semiconductor device of claim 82, wherein said at least one metal stack comprises a fourth metal.

85. (Previously presented) The semiconductor device of claim 84, wherein said fourth metal is gold.

86. (Previously presented) The semiconductor device of claim 76, wherein said second insulating layer is approximately 1.5 microns thick.